What is claimed is:

1. An arrangement of a plurality of integrated circuit devices including a first integrated circuit device driven by a first clock signal at a first clock rate, the arrangement comprising:

a parallel data bus coupled to communicate with the first integrated circuit device in response to the first clock signal;

a universal asynchronous receiver/transmitter (UART) chip including a serial communication circuit adapted to communicate serial data at a second rate defined by a second clock signal, a parallel bus interface circuit responsive to the first clock signal and adapted to pass data between the parallel data bus and the serial communication circuit, and a data-storage-register circuit adapted to output status data to the parallel data bus, the status data indicative of states of at least one of the serial communication circuit and the parallel bus interface circuit; and

a clock control circuit adapted to reduce the first clock rate in response to a clock control signal and therein provide a power-reduced UART mode in which the serial communication circuit is adapted to continue communication of serial data at the second rate.

2. The arrangement of claim 1, wherein the clock control circuit is further adapted to reduce the first clock rate to zero.

3. The arrangement of claim 1, wherein the clock control circuit is further adapted to reduce the first clock rate to a third clock rate that is at least ten percent slower than the first clock rate.

4. The arrangement of claim 1, wherein the second clock rate is derived from the first clock rate.

5. The arrangement of claim 1, wherein the first clock rate and the second clock rate change states asynchronously.

6. The arrangement of claim 1, wherein the second clock rate is set to define serial communication with another of the plurality of integrated circuit devices.

7. The arrangement of claim 1, wherein the UART chip further includes a first-in-first-out (FIFO) buffer adapted to store data passing between the serial communication circuit and the parallel bus interface circuit.

8. The arrangement of claim 1, wherein the data-storage-register circuit is further adapted to provide data indicative of at least one flow condition for data passing between the parallel data bus and the serial communication circuit.

9. The arrangement of claim 8, wherein said at least one flow condition include an overflow condition and an underflow condition.

10. The arrangement of claim 1, wherein the UART chip further includes a first-in-first-out (FIFO) buffer adapted to store data passing between the serial communication circuit and the parallel bus interface circuit, and wherein the data-storage-register circuit is further adapted to provide data indicative of at least one flow condition for data passing through the FIFO.